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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,862	04/12/2004	Angus Chen	3345/4 CIP	1809

23338 7590 09/16/2005

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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,862	CHEN ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *3-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed November 9, 2004 complies with all the requirements set forth in MPEP 602 and therefore is accepted.

Drawings

The drawings filed April 12, 2004 are accepted.

Specification

The specification filed April 12, 2004 is accepted.

Claim Objections

Claim 3 is objected to because of the following informalities:

- The claim depends on itself, which is improper.

Appropriate correction is required.

Allowable Subject Matter

Claims 3-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However the dependency correction to claim 3 would be eliminated if it is written in independent format.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The preamble of the claim is not clearly written. It states, "a pre-stored digital word generator is applied to a trigger signal generating of test channel of a chip tester..." which is not clear.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parker (USPN 5402427).

As per claim 1, Parker substantially teaches test connectors that connect a circuit tester to an electronic device to be tested. The test vector matrix is divided into segments, each segment including one or more columns of the matrix. The unique vector segments within each matrix

segment are stored in RAMs, one RAM for each test connector. A driver/comparator applies an electrical signal to some of the test connectors in response to a signal received from its associated RAM and receives an electrical signal on other of the test connectors and compares it to a signal received from the RAM. There is an independent sequencer for each matrix segment, each sequencer addressing the RAMs for that segment. A clock initiates and clocks the sequencers in synchrony to produce the test on the test connectors from the unique test vector segments stored in the RAMs.

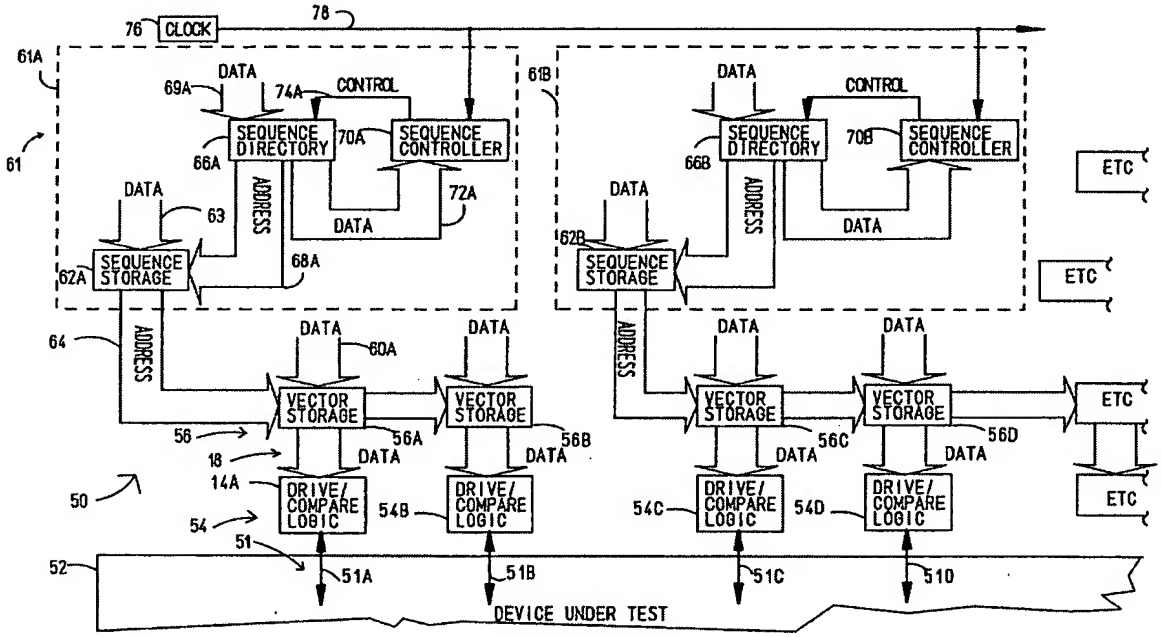

FIG 2

In particular, Parker teaches Figure 2 a circuit with a plurality of sequencers 61, such as 61A, 61B, etc., with each sequencer including a sequencer storage unit, such as 62A, a sequence directory unit, such as 66A, and a sequence controller, such as 70A. Each sequencer, such as 61A, is independent of the other sequencers 61 except for the common clock 76. Each

sequencer, such as 61A, and its associated vector storage units, such as 56A and 56B, store an independently compressed segment of the complete test. When all the sequencers 61 are initiated and clocked in synchrony by clock 76 so that they run coincidently, the complete test is generated.

Parker does not explicitly teach a separate edge address counter and a reloadable down counter as stated in the present application.

However, Parker teaches sequence controller 70 (Figure 2 and associated text) that controls the sequence directory and is electrically connected to it. The edge address counter and the reloadable down counter are used in the present application to trigger the addresses of the edge memory in sequence. The Examiner would like to point out that this functionality of the edge address counter and the reloadable down counter are taught by Parker. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an edge address counter and a reloadable down counter. This would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that the result of the edge address counter and the reloadable down counter would have been necessary for the proper addressing of the edge memory.

As per claim 2, Parker substantially teaches, in view of above rejections, (col. 2-4) dividing a test vector matrix into segments and compressing each matrix segment to the unique vector segments in of the matrix segments; storing each unique vector segment in one or more vector storage units; and sequencing the stored unique vector segments to produce a test corresponding to the test vector matrix on the electronic circuit. Preferably, the step of sequencing comprises storing the unique sequences of vector segments in each of the matrix

segments and applying the unique sequences to the vector storage units to produce the test. Preferably, the vector storage units comprise electronic storage devices with the unique vector segments stored at various addresses and the step of sequencing comprises applying the addresses corresponding to the unique sequences to the electronic storage devices to cause the electronic storage devices to output the sequences of the unique vector segments to produce the test. Preferably, there are a plurality of the vector storage units and the step of storing comprises dividing each unique vector segment into two or more portions and storing each portion in a different one of the vector storage units. The Examiner would like to point out that (table 1, cols. 4-5) shown a variety of signals.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts are included herein for Applicant's review.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2133
September 5, 2005

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
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